TA3020

STEREO 300W (4Ω) CLASS-T DIGITAL AUDIO AMPLIFIER DRIVER USING DIGITAL POWER PROCESSING (DPP™) TECHNOLOGY

Technical Information **Revision 2 – November 2001**

GENERAL DESCRIPTION

The TA3020 is a two-channel, 300W (4Ω) per channel Amplifier Driver IC that uses Tripath's proprietary Digital Power Processing (DPP™) technology. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

APPLICATIONS

- Audio/Video Amplifiers & Receivers
- Pro-audio Amplifiers
- Automobile Power Amplifiers
- Subwoofer Amplifiers

BENEFITS

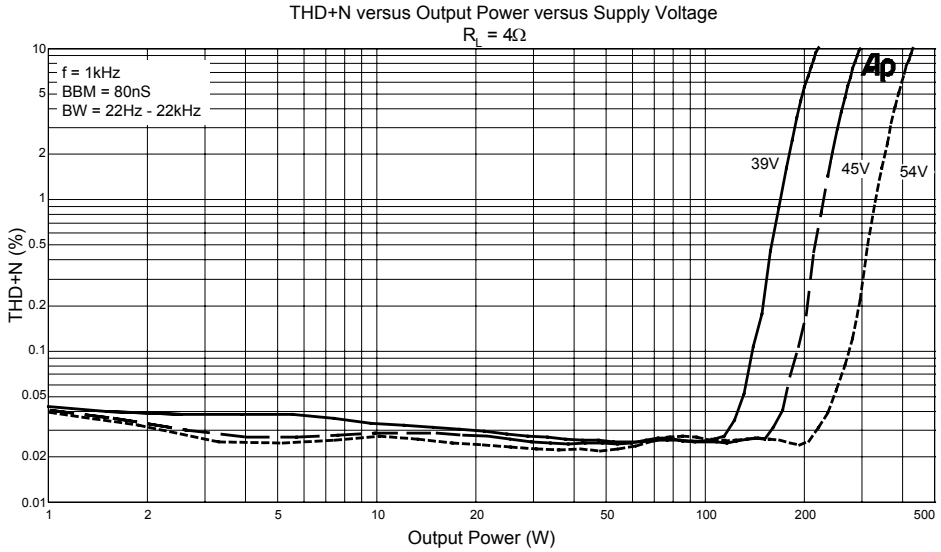
- Reduced system cost with smaller/less expensive power supply and heat sink
- Signal fidelity equal to high quality Class-AB amplifiers
- High dynamic range compatible with digital media such as CD and DVD

FEATURES

- Class-T architecture
- Proprietary Digital Power Processing technology
- "Audiophile" Sound Quality
  - 0.02% THD+N @ 50W, 8Ω
  - 0.03% IHF-IM @ 30W, 8Ω
- High Efficiency
  - 95% @ 150W @ 8Ω
  - 90% @ 275W @ 4Ω
- Supports wide range of output power levels
  - Up to 300W/channel (4Ω), single-ended outputs
  - Up to 1000W (4Ω), bridged outputs
- Output over-current protection
- Over- and under-voltage protection

48-pin DIP (dual-inline package)

TYPICAL PERFORMANCE



Absolute Maximum Ratings (Note 1)

SYMBOL	PARAMETER	Value	UNITS
VPP, VNN	Supply Voltage	+/- 70	V
V5	Positive 5 V Bias Supply Voltage at Input Pins (pins 12-16, 18, 19-26, 29-33, 37)	6 -0.3V to (V5+0.3V)	V
VN10	Voltage for FET drive	VNN+13	V
T_{STORE}	Storage Temperature Range	-55º to 150º	C
T_A	Operating Free-air Temperature Range (Note 2)	-40º to 85º	C
T_J	Junction Temperature	150º	C
ESD_{HB}	ESD Susceptibility – Human Body Model (Note 3) All pins	TBD	V
ESD_{MM}	ESD Susceptibility – Machine Model (Note 4) All pins	TBD	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. See the table below for Operating Conditions.
Note 2: This is a target specification. Characterization is still needed to validate this temperature range.
Note 3: Human body model, 100pF discharged through a 1.5KΩ resistor.
Note 4: Machine model, 220pF – 240pF discharged through all pins.

Operating Conditions (Note 5)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
VPP, VNN	Supply Voltage	+/- 15	+/-45	+/- 65	V
V5	Positive 5 V Bias Supply	4.5	5	5.5	V
VN10	Voltage for FET drive (Volts above VNN)	9	10	12	V

Note 5: Recommended Operating Conditions indicate conditions for which the device is functional. See Electrical Characteristics for guaranteed specific performance limits.

Electrical Characteristics (Note 6)

T_A = 25 °C. See Application/Test Circuit on page 7. Unless otherwise noted, the supply voltage is VPP=|VNN|=45V.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
I_q	Quiescent Current (No load, BBM0=1,BBM1=0, Mute = 0V)	VPP = +45V VNN = -45V V5 = 5V VN10 = 10V		90 90 45 200	 TBD TBD	mA mA mA mA
I_{MUTE}	Mute Supply Current (No load, Mute = 5V)	VPP = +45V VNN = -45V V5 = 5V VN10 = 10V		1 1 20 1	 TBD 	mA mA mA mA
V_{IH}	High-level input voltage (MUTE)		3.5			V
V_{IL}	Low-level input voltage (MUTE)				1.0	V
V_{OH}	High-level output voltage (HMUTE)	I_{OH} = 3mA	4.0			V
V_{OL}	Low-level output voltage (HMUTE)	I_{OL} = 3mA			0.5	V
V_{OFFSET}	Output Offset Voltage	No Load, MUTE = Logic low 0.1% R_{FBA}, R_{FBB}, R_{FBC} resistors	-TBD		TBD	mV
I_{OC}	Over Current Sense Voltage Threshold	TBD	TBD	1.0	TBD	V
$I_{VPPSENSE}$	VPPSENSE Threshold Currents	Over-voltage turn on (muted) Over-voltage turn off (mute off) Under-voltage turn off (mute off) Under-voltage turn on (muted)	 TBD TBD	162 154 79 72	TBD TBD 	µA µA µA µA
$V_{VPPSENSE}$	Threshold Voltages with $R_{VPPSENSE}$ = XXKΩ	Over-voltage turn on (muted) Over-voltage turn off (mute off) Under-voltage turn off (mute off) Under-voltage turn on (muted)	 TBD TBD	TBD TBD TBD TBD	TBD TBD 	V V V V
$I_{VNNSENSE}$	VNNSENSE Threshold Currents	Over-voltage turn on (muted) Over-voltage turn off (mute off) Under-voltage turn off (mute off) Under-voltage turn on (muted)	 TBD TBD	174 169 86 77	TBD TBD 	µA µA µA µA
$V_{VNNSENSE}$	Threshold Voltages with $R_{VNNSENSE}$ = XXKΩ	Over-voltage turn on (muted) Over-voltage turn off (mute off) Under-voltage turn off (mute off) Under-voltage turn on (muted)	 TBD TBD	TBD TBD TBD TBD	TBD TBD 	V V V V

Note 6: Minimum and maximum limits are guaranteed but may not be 100% tested.

Note 7: These supply voltages are calculated using the IVPPSENSE and IVNNSENSE values shown in the Electrical Characteristics table. The typical voltage values shown are calculated using a RVPPSENSE and RVNNSENSE value of 422kohm without any tolerance variation. The minimum and maximum voltage limits shown include either a +1% or –1% (+1% for Over-voltage turn on and Under-voltage turn off, -1% for Over-voltage turn off and Under-voltage turn on) variation of RVPPSENSE or RVNNSENSE off the nominal 422kohm and 392kohm values. These voltage specifications are examples to show both typical and worst case voltage ranges for a given RVPPSENSE and RVNNSENSE resistor values of 422kohm and 392kohm. Please refer to the Application Information section for a more detailed description of how to calculate the over and under voltage trip voltages for a given resistor value.

Note 8: The fact that the over-voltage turn on specifications exceed the absolute maximum of +/-70V for the TA3020 does not imply that the part will work at these elevated supply voltages. It also does not imply that the TA3020 is tested or guaranteed at these supply voltages. The supply voltages are simply a calculation based on the process spread of the IVPPSENSE and IVNNSENSE currents (see note 7). The supply voltage must be maintained below the absolute maximum of +/-70V or permanent damage to the TA3020 may occur.

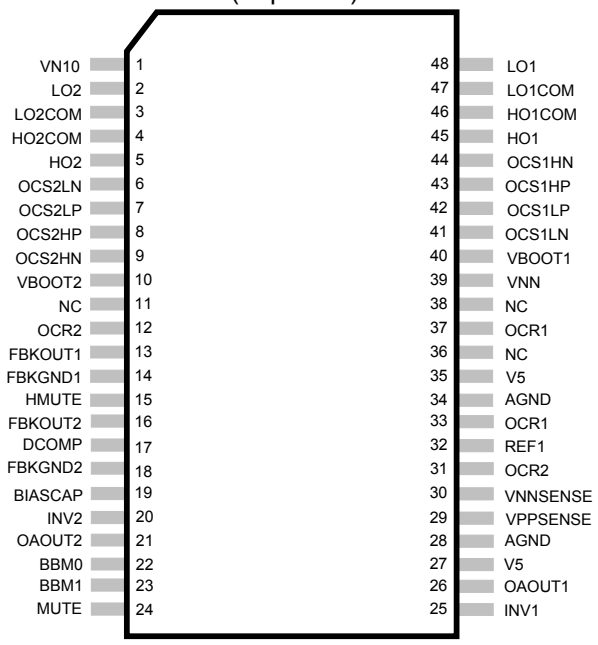
Performance Characteristics – Single Ended

T_A = 25 °C. Unless otherwise noted, the supply voltage is VPP=|VNN|=45V, the input frequency is 1kHz and the measurement bandwidth is 20kHz. See Application/Test Circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
P_{OUT}	Output Power (continuous RMS/Channel)	THD+N = 0.1%, R_L = 8Ω R_L = 4Ω THD+N = 1%, R_L = 8Ω R_L = 4Ω		100 190 120 220		W W W W
THD + N	Total Harmonic Distortion Plus Noise	P_{OUT} = 50W/Channel, R_L = 8Ω		0.02		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF), R_L = 8Ω P_{OUT} = 30W/Channel		0.03		%
SNR	Signal-to-Noise Ratio	A Weighted, R_L = 4Ω, P_{OUT} = 275W/Channel		102		dB
CS	Channel Separation	0dBr = 30W, R_L = 8Ω, f = 1kHz		97		dB
η	Power Efficiency	P_{OUT} = 150W/Channel, R_L = 8Ω		95		%
A_V	Amplifier Gain	P_{OUT} = 10W/Channel, R_L = 4Ω See Application / Test Circuit		TBD		V/V
A_{VERROR}	Channel to Channel Gain Error	P_{OUT} = 10W/Channel, R_L = 4Ω See Application / Test Circuit			0.5	dB
e_{NOUT}	Output Noise Voltage	A Weighted, no signal, input shorted, DC offset nulled to zero		260		μV

TA3020 Pinout

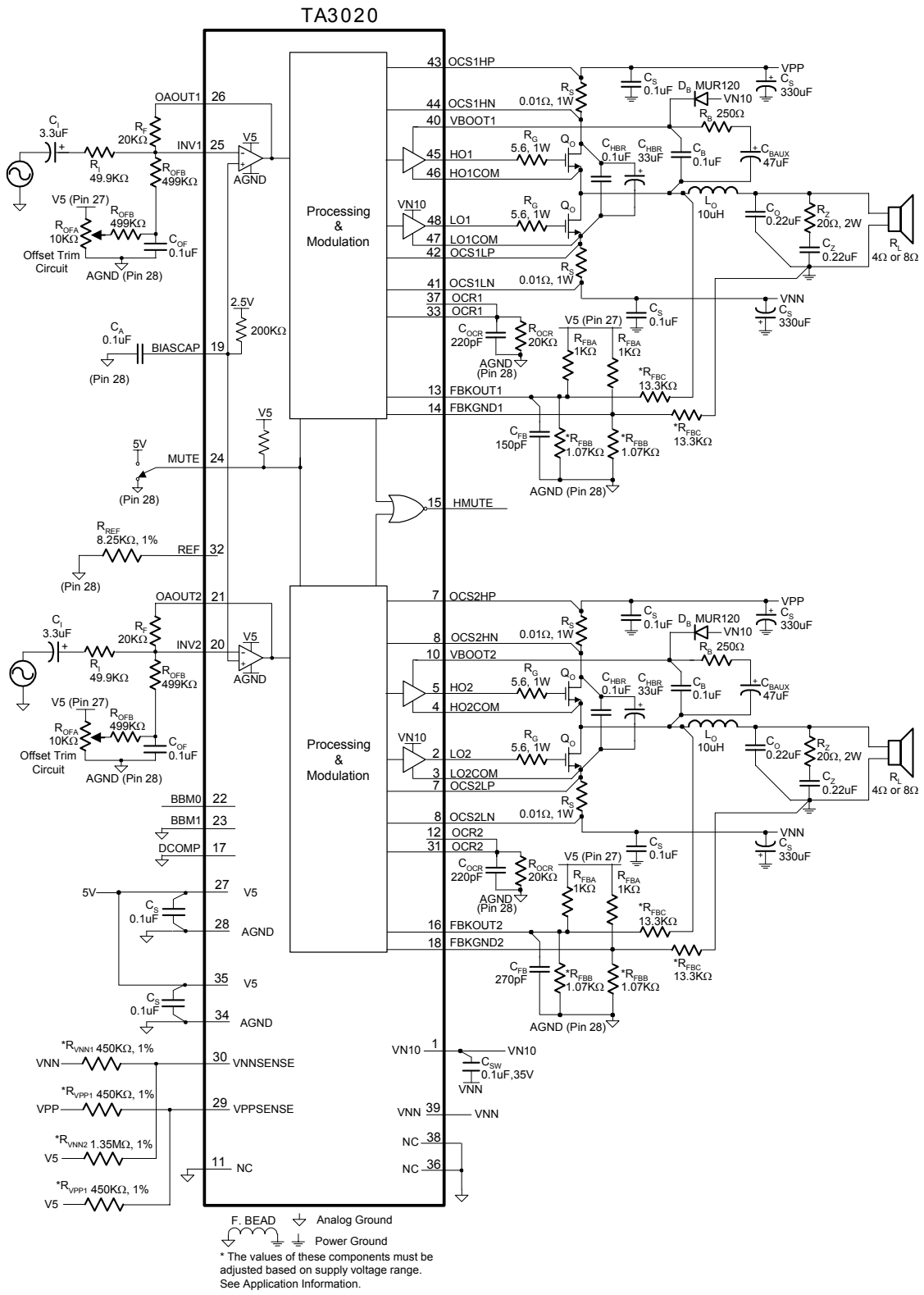
48-pin Dip
(Top View)



Pin Description

Pin	Function	Description
1	VN10	"Floating" supply input for the FET drive circuitry. This voltage must be stable and referenced to VNN.
2,48	LO2, LO1	Low side gate drive output (Channel 2 & 1)
3,47	LO2COM, LO1COM	Kelvin connection to source of low-side transistor (Channel 2 & 1)
4,46	HO2COM, HO1COM	Kelvin connection to source of high-side transistor (Channel 2 & 1)
5,45	HO2, HO1	High side gate drive output (Channel 2 & 1)
6, 7	OCS2LN, OCS2LP	Over Current Sense inputs, Channel 2 low-side
8, 9	OCS2HP, OCS2HN	Over Current Sense inputs, Channel 2 high-side
10, 40	VBOOT2, VBOOT1	Bootstrapped voltage to supply drive to gate of high-side FET (Channel 2 & 1)
12, 31	OCR2	Over-current threshold adjustment (Channel 2)
13, 16	FBKOUT1, FBKOUT2	Switching feedback (Channels 1 & 2)
14, 18	FBKGND1, FBKGND2	Ground Kelvin feedback (Channels 1 & 2)
15	HMUTE	Logic Output. A logic high indicates both amplifiers are muted, due to the mute pin state, or a "fault" such as an overcurrent, undervoltage, or overvoltage condition.
17	DCOMP	Internal mode selection. This pin must be grounded for proper device operation.
19	BIASCAP	Bandgap reference times two (typically 2.5VDC). Used to set the common mode voltage for the input op amps. This pin is not capable of driving external circuitry.
20, 25	INV2, INV1	Inverting inputs of Input Stage op amps. (Channels 2 & 1)
21, 26	OAOUT2, OAOUT1	Outputs of Input Stage op amps. (Channels 2 & 1)
22, 23	BBM0, BBM1	Break-before-make timing control to prevent shoot-through in the output FETs.
24	MUTE	Logic input. A logic high puts the amplifier in mute mode. Ground pin if not used. Please refer to the section, Mute Control, in the Application Information.
27, 35	V5	5V power supply input.
28,34	AGND	Analog ground.
29	VPPSENSE	Positive supply voltage sense input. This pin is used for both over and under voltage sensing for the VPP supply.
30	VNNSENSE	Negative supply voltage sense input. This pin is used for both over and under voltage sensing for the VNN supply.
32	REF	Used to set internal bias currents. The pin voltage is typically 1.1V.
33, 37	OCR1	Over-current threshold adjustment (Channel 1)
39	VNN	Negative supply voltage.
41, 42	OCS1LN, OCS1LP	Over Current Sense inputs, Channel 1 low-side
43, 44	OCS1HP, OCS1HN	Over Current Sense inputs, Channel 1 high-side
11, 36, 38	NC	Not connected (bonded) internally. To minimize coupling between pins, tie these pins to AGND (pin34).

Application/Test Circuit



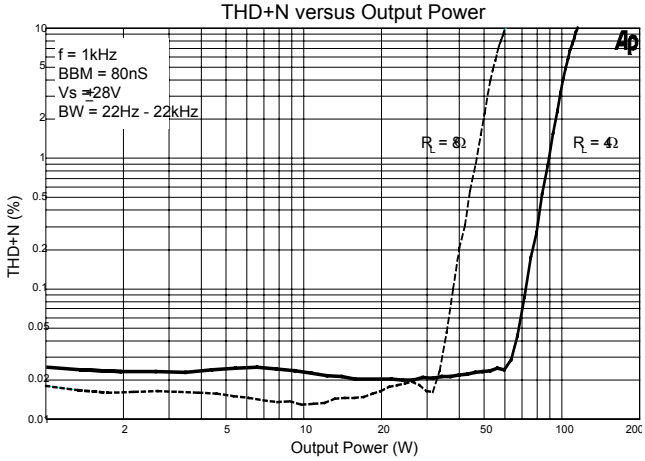
External Components Description (Refer to the Application/Test Circuit)

Components	Description
R_I	Inverting input resistance to provide AC gain in conjunction with R_F. This input is biased at the BIASCAP voltage (approximately 2.5VDC).
R_F	Feedback resistor to set AC gain in conjunction with R_I. Please refer to the Amplifier Gain paragraph, in the Application Information section.
C_I	AC input coupling capacitor which, in conjunction with R_I, forms a highpass filter at $f_C = 1/(2\pi R_I C_I)$.
R_{FBA}	Feedback divider resistor connected to V5. This resistor is normally set at 1kΩ.
R_{FBB}	Feedback divider resistor connected to AGND. This value of this resistor depends on the supply voltage setting and helps set the TA3020 gain in conjunction with R_I, R_F, R_{FBA}, and R_{FBC}. Please see the Modulator Feedback Design paragraphs in the Application Information Section.
R_{FBC}	Feedback resistor connected from either the OUT1(OUT2) to FBKOUT1(FBKOUT2) or speaker ground to FBKGND1(FBKGND2). The value of this resistor depends on the supply voltage setting and helps set the TA3020 gain in conjunction with R_I, R_F, R_{FBA}, and R_{FBB}. It should be noted that the resistor from OUT1(OUT2) to FBKOUT1(FBKOUT2) must have a power rating of greater than $P_{DISS} = VPP^2/(2R_{FBC})$. Please see the Modulator Feedback Design paragraphs in the Application Information Section.
C_{FB}	Feedback delay capacitor that both lowers the idle switching frequency and filters very high frequency noise from the feedback signal, which improves amplifier performance. The value of C_{FB} should be offset between channel 1 and channel 2 so that the idle switching difference is greater than 40kHz. Please refer to the Application / Test Circuit.
R_{OFA}	Potentiometer used to manually trim the DC offset on the output of the TA3020.
R_{OFB}	Resistor that limits the manual DC offset trim range and allows for more precise adjustment.
R_{REF}	Bias resistor. Locate close to pin 32 and ground at pin 28.
C_A	BIASCAP decoupling capacitor. Should be located close to pin 19 and grounded at pin 28.
D_B	Bootstrap diode. This diode charges up the bootstrap capacitors when the output is low (at VNN) to drive the high side gate circuitry. A fast or ultra fast recovery diode is recommended for the bootstrap circuitry. In addition, the bootstrap diode must be able to sustain the entire VPP-VNN voltage. Thus, for most applications, a 150V (or greater) diode should be used.
C_B	High frequency bootstrap capacitor, which filters the high side gate drive supply. This capacitor must be located as close to pin 40 (VBOOT1) or pin10 (VBOOT2) for reliable operation. The “negative” side of C_B should be connected directly to the HO1COM (pin 46) or HO2COM (pin 4). Please refer to the Application / Test Circuit.
C_{BAUX}	Bulk bootstrap capacitor that supplements C_B during “clipping” events, which result in a reduction in the average switching frequency.
R_B	Bootstrap resistor that limits C_{BAUX} charging current during TA3020 power up (bootstrap supply charging).
C_{SW}	VN10 generator filter capacitors. The high frequency capacitor (0.1uF) must be located close to pin 1 (VN10) to maximize device performance.
C_S	Supply decoupling for the power supply pins. For optimum performance, these components should be located close to the TA3020 and returned to their respective ground as shown in the Application/Test Circuit.
R_{VNN1}	Main overvoltage and undervoltage sense resistor for the negative supply (VNN). Please refer to the Electrical Characteristics Section for the trip points as well as the hysteresis band. Also, please refer to the Over / Under-voltage Protection section in the Application Information for a detailed discussion of the internal circuit operation and external component selection.
R_{VNN2}	Secondary overvoltage and undervoltage sense resistor for the negative supply (VNN). This resistor accounts for the internal $V_{NNSENSE}$ bias of 1.25V. Nominal resistor value should be three times that of R_{VNN1}. Please refer to the Over / Under-voltage Protection section in the Application Information for a detailed discussion of

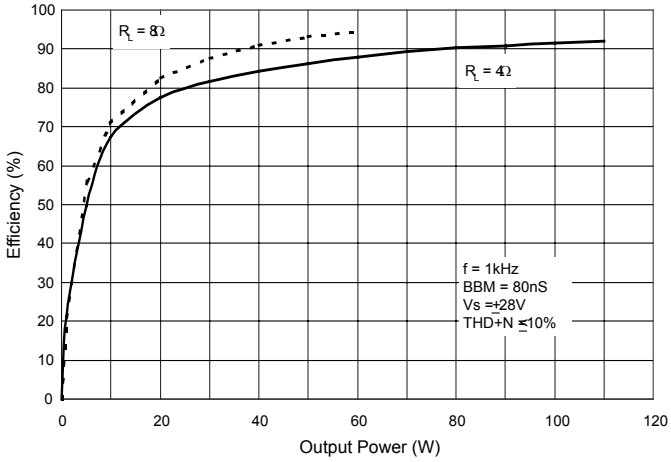
	the internal circuit operation and external component selection.
R_{VPP1}	Main overvoltage and undervoltage sense resistor for the positive supply (VPP). Please refer to the Electrical Characteristics Section for the trip points as well as the hysteresis band. Also, please refer to the Over / Under-voltage Protection section in the Application Information for a detailed discussion of the internal circuit operation and external component selection.
R_{VPP2}	Secondary overvoltage and undervoltage sense resistor for the positive supply (VPP). This resistor accounts for the internal $V_{PPSENSE}$ bias of 2.5V. Nominal resistor value should be equal to that of R_{VPP1}. Please refer to the Over / Under-voltage Protection section in the Application Information for a detailed discussion of the internal circuit operation and external component selection.
R_S	Over-current sense resistor. Please refer to the section, Setting the Over-current Threshold, in the Application Information for a discussion of how to choose the value of R_S to obtain a specific current limit trip point.
R_{OCR}	Over-current "trim" resistor, which, in conjunction with R_S, sets the current trip point. Please refer to the section, Setting the Over-current Threshold, in the Application Information for a discussion of how to calculate the value of R_{OCR}.
C_{OCR}	Over-current filter capacitor, which filters the overcurrent signal at the OCR pins to account for the half-wave rectified current sense circuit internal to the TA3020. A typical value for this component is 220pF. In addition, this component should be located near pin 31 or pin 33 as possible.
C_{HBR}	Supply decoupling for the high current Half-bridge supply pins. These components must be located as close to the output MOSFETs as possible to minimize output ringing which causes power supply overshoot. By reducing overshoot, these capacitors maximize both the TA3020 and output MOSFET reliability. These capacitors should have good high frequency performance including low ESR and low ESL. In addition, the capacitor rating must be twice the maximum VPP voltage. Panasonic EB capacitors are ideal for the bulk storage (nominally 33uF) due to their high ripple current and high frequency design.
R_G	Gate resistor, which is used to control the MOSFET rise/ fall times. This resistor serves to dampen the parasitics at the MOSFET gates, which, in turn, minimizes ringing and output overshoots. The typical power rating is 1 watt.
C_Z	Zobel capacitor, which in conjunction with R_Z, terminates the output filter at high frequencies. Use a high quality film capacitor capable of sustaining the ripple current caused by the switching outputs.
R_Z	Zobel resistor, which in conjunction with C_Z, terminates the output filter at high frequencies. The combination of R_Z and C_Z minimizes peaking of the output filter under both no load conditions or with real world loads, including loudspeakers which usually exhibit a rising impedance with increasing frequency. Depending on the program material, the power rating of R_Z may need to be adjusted. The typical power rating is 2 watts.
L_O	Output inductor, which in conjunction with C_O, demodulates (filters) the switching waveform into an audio signal. Forms a second order filter with a cutoff frequency of $f_C = 1/(2\pi\sqrt{L_O C_O})$ and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$.
C_O	Output capacitor, which, in conjunction with L_O, demodulates (filters) the switching waveform into an audio signal. Forms a second order low-pass filter with a cutoff frequency of $f_C = 1/(2\pi\sqrt{L_O C_O})$ and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$. Use a high quality film capacitor capable of sustaining the ripple current caused by the switching outputs.

Typical Performance

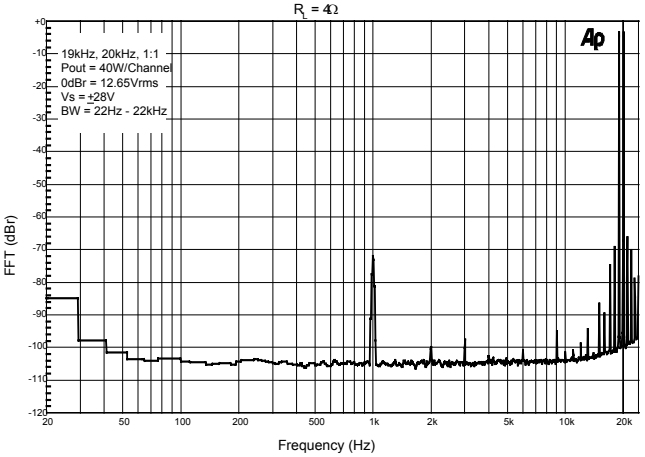
THD+N versus Output Power



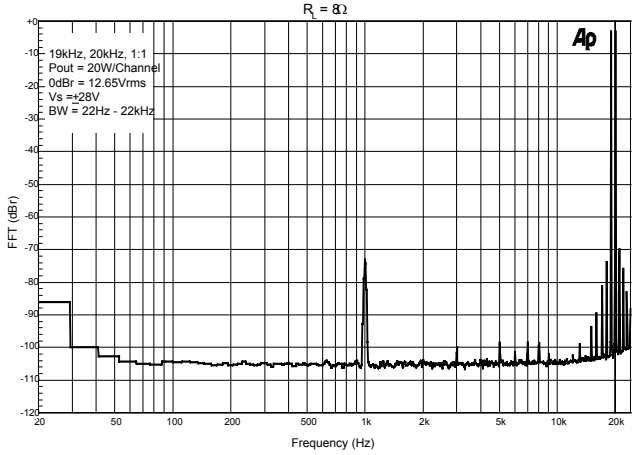
Efficiency versus Output Power



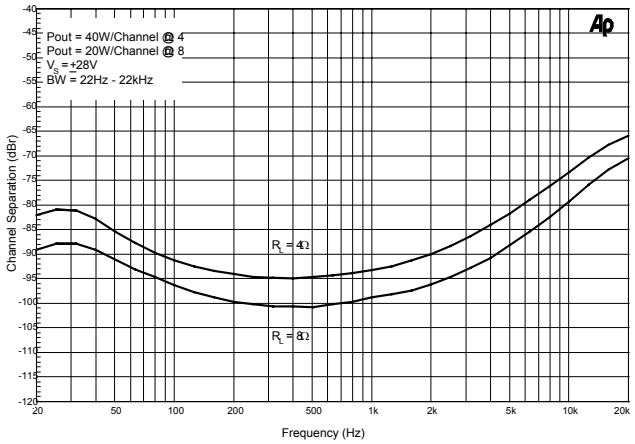
Intermodulation Performance
RL = 4Ω



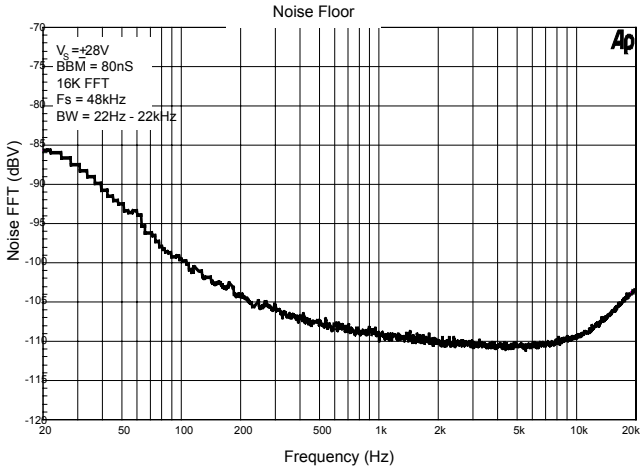
Intermodulation Performance
RL = 8Ω



Channel Separation versus Frequency

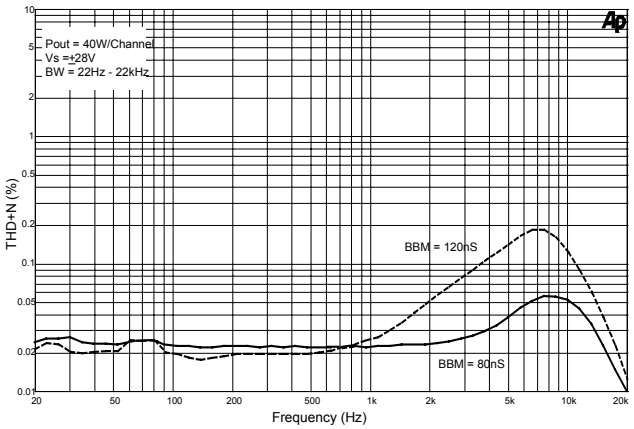


Noise Floor

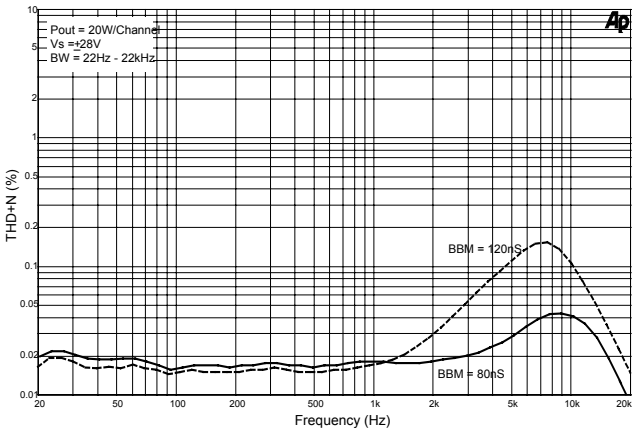


Typical Performance

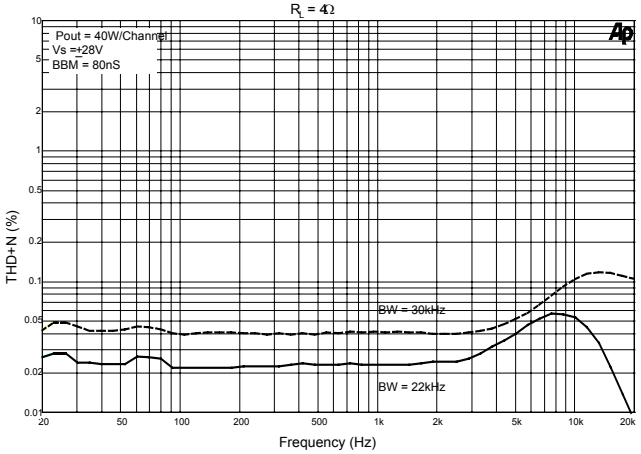
THD+N versus Frequency versus Break Before Make
R_L = 4Ω



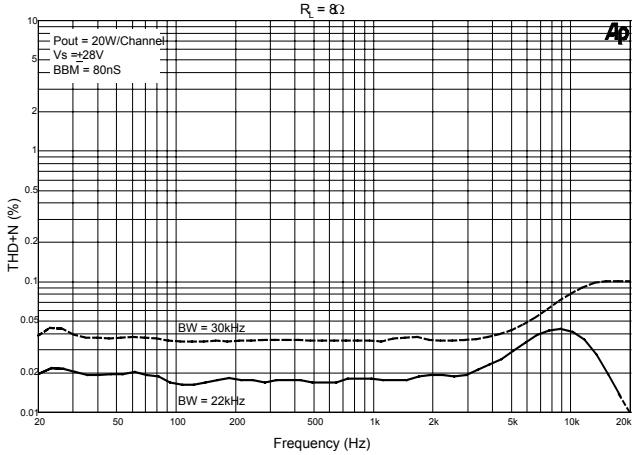
THD+N versus Frequency versus Break Before Make
R_L = 8Ω



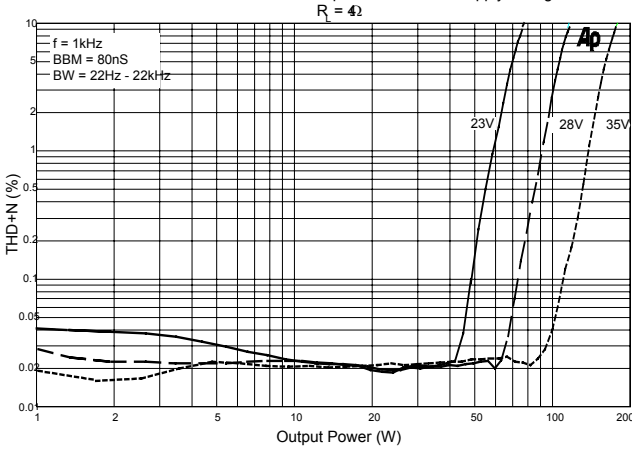
THD+N versus Frequency versus Bandwidth
R_L = 4Ω



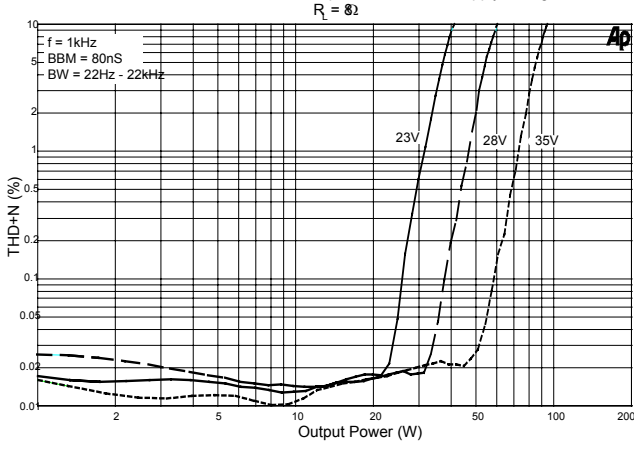
THD+N versus Frequency versus Bandwidth
R_L = 8Ω



THD+N versus Output Power versus Supply Voltage
R_L = 4Ω

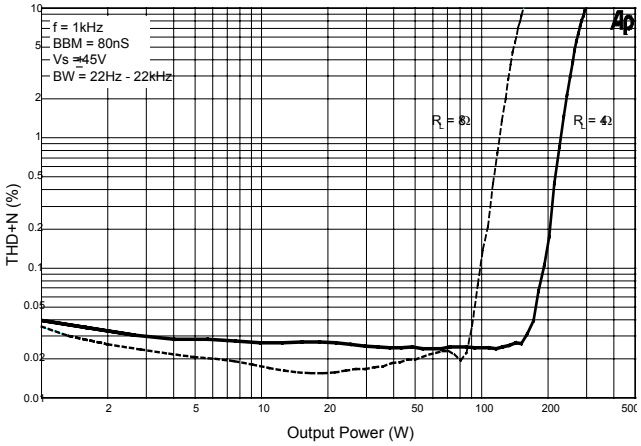


THD+N versus Output Power versus Supply Voltage
R_L = 8Ω

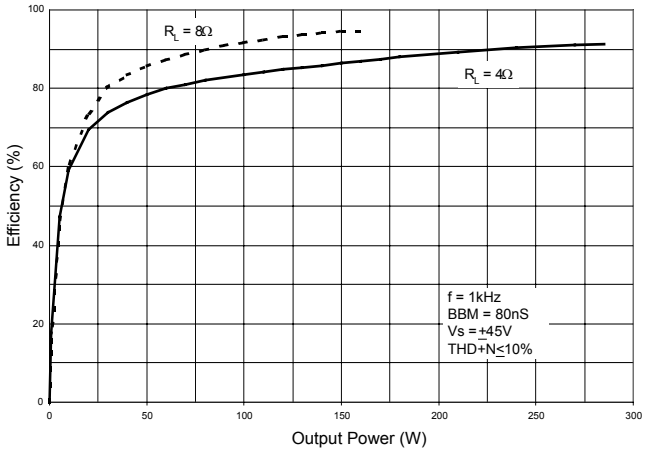


Typical Performance

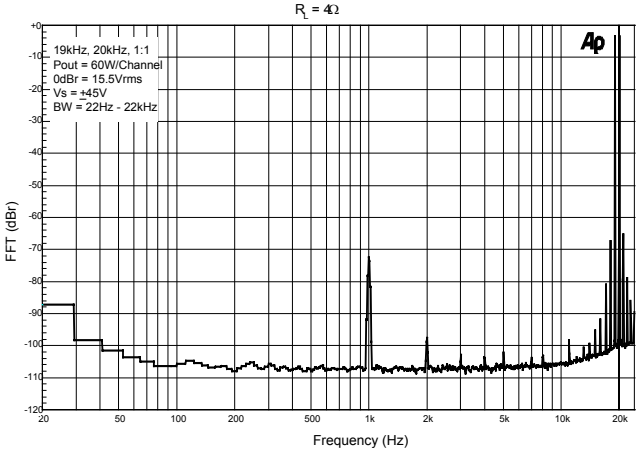
THD+N versus Output Power



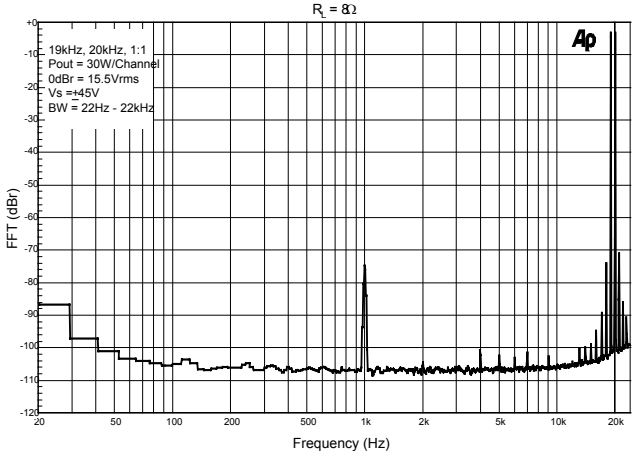
Efficiency versus Output Power



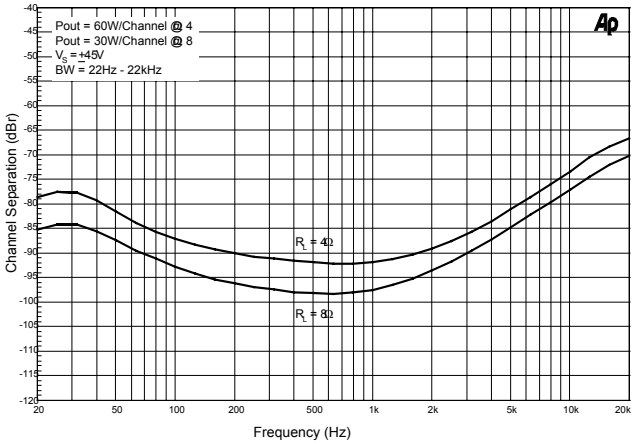
Intermodulation Performance
RL = 4Ω



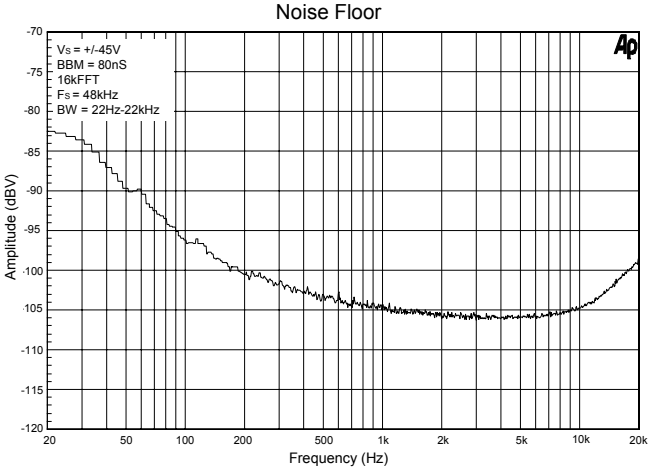
Intermodulation Performance
RL = 8Ω



Channel Separation versus Frequency

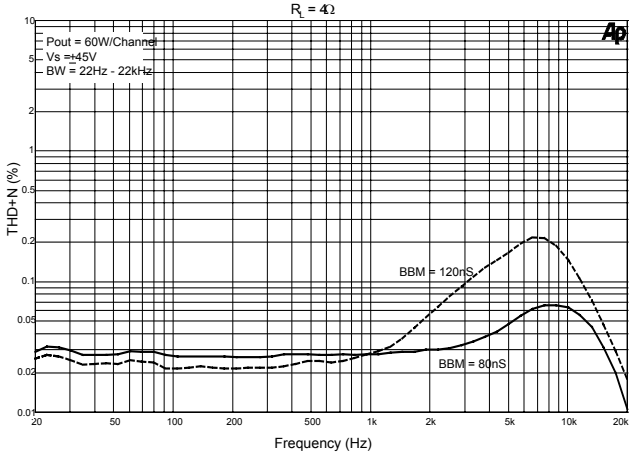


Noise Floor

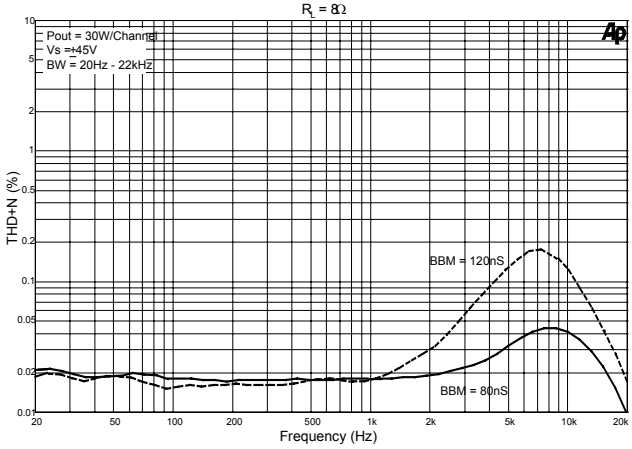


Typical Performance

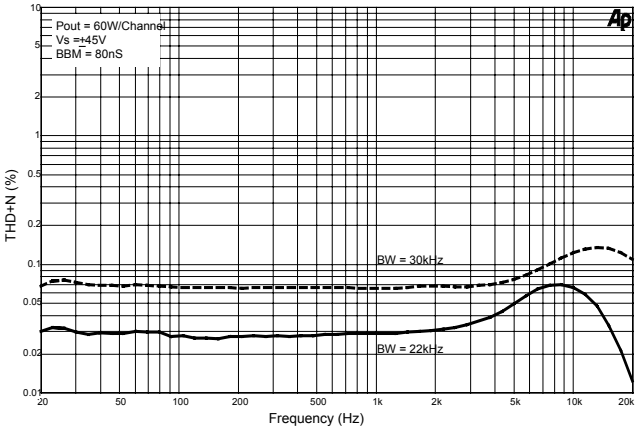
THD+N versus Frequency versus Break Before Make
R_L = 4Ω



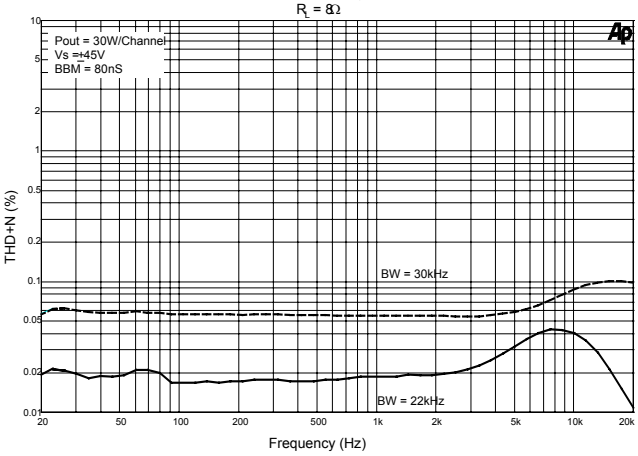
THD+N versus Frequency versus Break Before Make
R_L = 8Ω



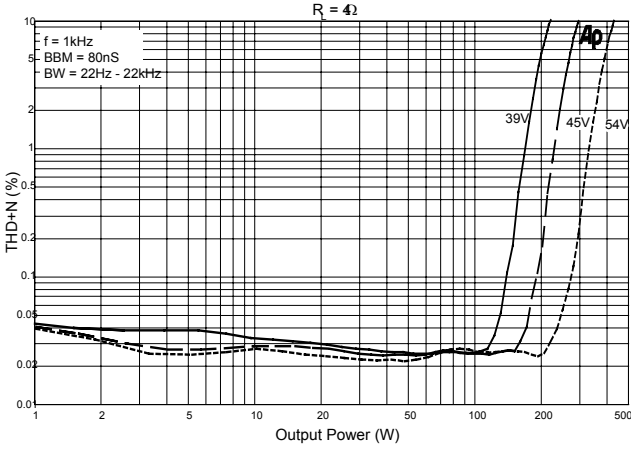
THD+N versus Frequency versus Bandwidth
R_L = 4Ω



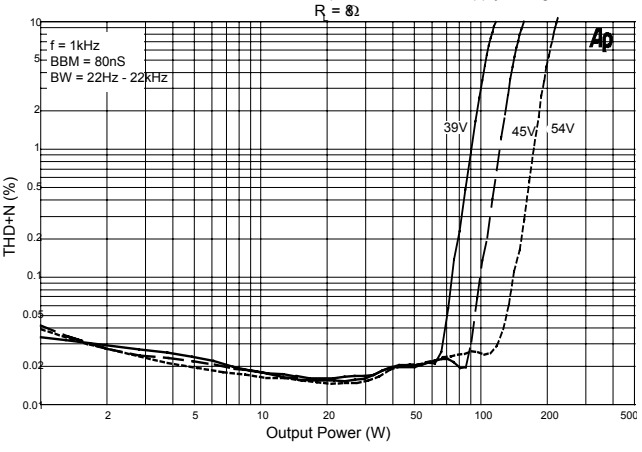
THD+N versus Frequency versus Bandwidth
R_L = 8Ω



THD+N versus Output Power versus Supply Voltage
R_L = 4Ω



THD+N versus Output Power versus Supply Voltage
R_L = 8Ω



Application Information

Figure 1 is a simplified diagram of one channel (Channel 1) of a TA3020 amplifier to assist in understanding its operation.

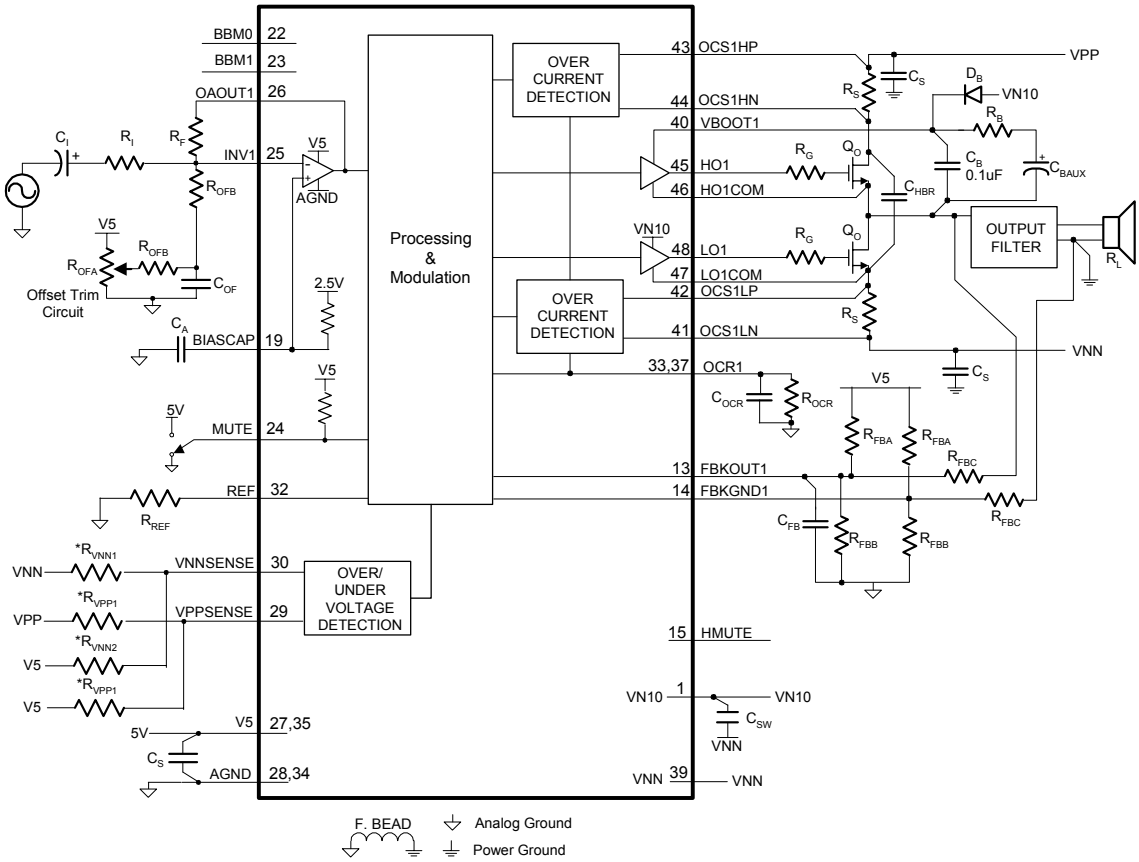


Figure 1: Simplified TA3020 Amplifier

TA3020 Basic Amplifier Operation

The audio input signal is fed to the processor internal to the TA3020, where a switching pattern is generated. The average idle (no input) switching frequency is approximately 700kHz. With an input signal, the pattern is spread spectrum and varies between approximately 200kHz and 1.5MHz depending on input signal level and frequency. Complementary copies of the switching pattern are level-shifted by the MOSFET drivers and output from the TA3020 where they drive the gates (HO1 and LO1) of external power MOSFETs that are connected as a half bridge. The output of the half bridge is a power-amplified version of the switching pattern that switches between VPP and VNN. This signal is then low-pass filtered to obtain an amplified reproduction of the audio input signal.

The processor portion of the TA3020 is operated from a 5-volt supply. In the generation of the switching patterns for the output MOSFETs, the processor inserts a “break-before-make” dead time between the turn-off of one transistor and the turn-on of the other in order to minimize shoot-through currents in the MOSFETs. The dead time can be programmed by setting the break-before-make control bits, BBM1 and BBM0. Feedback information from the output of the half-bridge is supplied to the processor via FBKOUT1. Additional feedback information to account for ground bounce is supplied via FBKGND1.

The MOSFET drivers in the TA3020 are operated from voltages obtained from VN10 and LO1COM for the low-side driver, and VBOOT1 and HO1COM for the high-side driver. VN10 must be a regulated 10V above VNN.

N-Channel MOSFETs are used for both the top and bottom of the half bridge. The gate resistors, R_G, are used to control MOSFET slew rate and thereby minimize voltage overshoots.

Circuit Board Layout

The TA3020 is a power (high current) amplifier that operates at relatively high switching frequencies. The output of the amplifier switches between VPP and VNN at high speeds while driving large currents. This high-frequency digital signal is passed through an LC low-pass filter to recover the amplified audio signal. Since the amplifier must drive the inductive LC output filter and speaker loads, the amplifier outputs can be pulled above the supply voltage and below ground by the energy in the output inductance. To avoid subjecting the TA3020 to potentially damaging voltage stress, it is critical to have a good printed circuit board layout. It is recommended that Tripath's layout and application circuit be used for all applications and only be deviated from after careful analysis of the effects of any changes. Please refer to the TA3020 evaluation board document, EB-TA3020, available on the Tripath website, at www.tripath.com.

The following components are important to place near either their associated TA3020 or output MOSFET pins. The recommendations are ranked in order of layout importance, either for proper device operation or performance considerations.

- The capacitors, $C_{HBR,}$ provide high frequency bypassing of the amplifier power supplies and will serve to reduce spikes across the supply rails. Please note that both mosfet half-bridges must be decoupled separately. In addition, the voltage rating for C_{HBR} should be at least 150V as this capacitor is exposed to the full supply range, VPP-VNN.

- C_{FB} removes very high frequency components from the amplifier feedback signals and lowers the output switching frequency by delaying the feedback signals. In addition, the value of C_{FB} is different for channel 1 and channel 2 to keep the average switching frequency difference greater than 40kHz. This minimizes in-band audio noise. Locate these capacitors as close to their respective TA3020 pin as possible.

- To minimize noise pickup and minimize THD+N, R_{FBC} should be located as close to the TA3020 as possible. Make sure that the routing of the high voltage feedback lines is kept far away from the input op amps or significant noise coupling may occur. It is best to shield the high voltage feedback lines by using a ground plane around these traces as well as the input section.

- C_B, C_{SW} provides high frequency bypassing for the VN10 and bootstrap supplies. Very high currents are present on these supplies.

In general, to enable placement as close to the TA3020, and minimize PCB parasitics, the capacitors C_{FB}, C_B and C_{SW} should be surface mount types, located on the "solder" side of the board.

Some components are not sensitive to location but are very sensitive to layout and trace routing.

- To maximize the damping factor and reduce distortion and noise, the modulator feedback connections should be routed directly to the pins of the output inductors. L_O. Please refer to the EB-TA3020This was done on the EB-TA3020 for additional information.

- The output filter capacitor, C_O, and zobel capacitor, C_Z, should be star connected with the load return. The output ground feedback signal should be taken from this star point.

- The modulator feedback resistors, R_{FBA}, R_{FBB}, and $R_{FBC,}$ should all be grounded and attached to 5V together. These connections will serve to minimize common mode noise via the differential feedback. Please refer to the EB-TA3020 evaluation board for more information.

- The feedback signals that come directly from the output inductors are high voltage and high frequency in nature. If they are routed close to the input nodes, INV1 and INV2, the high impedance inverting opamp pins will pick up noise. This coupling will result in significant background noise, especially when the input is AC coupled to ground, or an external source such as a CD player or signal generator is connected. Thus, care should be taken such that the feedback lines are not routed near any of the input section.

- To minimize the possibility of any noise pickup, the trace lengths of INV1 and INV2 should be kept as short as possible. This is most easily accomplished by locating the input resistors, R_I and the input stage feedback resistors, R_F as close to the TA3020 as possible. In addition, the offset trim resistor, R_{OFB}, which connects to either INV1,or INV2, should be located close to the TA3020 input section.

TA3020 Grounding

Proper grounding techniques are required to maximize TA3020 functionality and performance. Parametric parameters such as THD+N, Noise Floor and Crosstalk can be adversely affected if proper grounding techniques are not implemented on the PCB layout. The following discussion highlights some recommendations about grounding both with respect to the TA3020 as well as general “audio system” design rules.

The TA3020 is divided into two sections: the input section, which spans pin 12 through pin 37, and the output (high voltage) section, which spans pin 1 through pin 10 and pin 39 through pin 48. On the TA3020 evaluation board, the ground is also divided into distinct sections, one for the input and one for the output. To minimize ground loops and keep the audio noise floor as low as possible, the input and output ground must be only connected at a single point. Depending on the system design, the single point connection may be in the form of a ferrite bead or a PCB trace.

The analog grounds, pin 28 and pin 34 must be connected locally at the TA3020 for proper device functionality. The ground for the V5 power supply should connect directly to pin 28. Additionally, any external input circuitry such as preamps, or active filters, should be referenced to pin 28.

For the power section, Tripath has traditionally used a “star” grounding scheme. Thus, the load ground returns and the power supply decoupling traces are routed separately back to the power supply. In addition, any type of shield or chassis connection would be connected directly to the ground star located at the power supply. These precautions will both minimize audible noise and enhance the crosstalk performance of the TA3020.

The TA3020 incorporates a differential feedback system to minimize the effects of ground bounce and cancel out common mode ground noise. As such, the feedback from the output ground for each channel needs to be properly sensed. This can be accomplished by connecting the output ground “sensing” trace directly to the star formed by the output ground return, output capacitor, C_O, and the zobel capacitor, C_Z. Refer to the Application / Test Circuit for a schematic description.

TA3020 Amplifier Gain

The gain of the TA3020 is the product of the input stage gain and the modulator gain. Please refer to the sections, Input Stage Design, and Modulator Feedback Design, for a complete explanation of how to determine the external component values.

$$A_{VTA3020} = A_{VINPUTSTAGE} * A_{V\,MODULATOR}$$

$$A_{VTA3020} \approx -\frac{R_F}{R_I}\left(\frac{R_{FBC} * (R_{FBA} + R_{FBB})}{R_{FBA} * R_{FBB}} + 1\right)$$

For example, using a TA3020 with the following external components,

R_I = 20kΩ
R_F = 20kΩ
R_{FBA} = 1kΩ
R_{FBB} = 1.13kΩ
R_{FBC} = 9.09kΩ

$$A_{VTA3020} \approx -\frac{20k\,\Omega}{49.9k\,\Omega}\left(\frac{13.3k\,\Omega * (1.0k\,\Omega + 1.07k\,\Omega)}{1.0k\,\Omega * 1.07k\,\Omega} + 1\right) = -10.71\,\frac{V}{V}$$

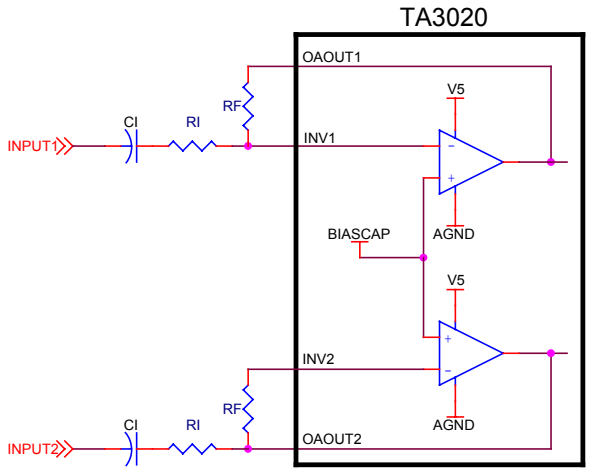
Input Stage Design

The TA3020 input stage is configured as an inverting amplifier, allowing the system designer flexibility in setting the input stage gain and frequency response. Figure 2 shows a typical application where the input stage is a constant gain inverting amplifier. The input stage gain should be set so that the maximum input signal level will drive the input stage output to 4Vpp.

The gain of the input stage, above the low frequency high pass filter point, is that of a simple inverting amplifier:

$$A_{VINPUTSTAGE} = -\frac{R_F}{R_I}$$

Figure 2: Input Stage



Input Capacitor Selection

C_{IN} can be calculated once a value for R_{IN} has been determined. C_{IN} and R_{IN} determine the input low-frequency pole. Typically this pole is set at 10Hz. C_{IN} is calculated according to:

$$C_{IN} = 1 / (2\pi \times F_P \times R_{IN})$$

where: R_{IN} = Input resistor value in ohms
F_P = Input low frequency pole (typically 10Hz)

Modulator Feedback Design

The modulator converts the signal from the input stage to the high-voltage output signal. The optimum gain of the modulator is determined from the maximum allowable feedback level for the modulator and maximum supply voltages for the power stage. Depending on the maximum supply voltage, the feedback ratio will need to be adjusted to maximize performance. The values of R_{FBA}, R_{FBB} and R_{FBC} (see explanation below) define the gain of the modulator. Once these values are chosen, based on the maximum supply voltage, the gain of the modulator will be fixed even with as the supply voltage fluctuates due to current draw.

For the best signal-to-noise ratio and lowest distortion, the maximum modulator feedback voltage should be approximately 4Vpp. This will keep the gain of the modulator as low as possible and still allow headroom so that the feedback signal does not clip the modulator feedback stage.

Figure 3 shows how the feedback from the output of the amplifier is returned to the input of the modulator. The input to the modulator (FBKOUT1/FBKGND1 for channel 1) can be viewed as inputs to an inverting differential amplifier. R_{FBA} and R_{FBB} bias the feedback signal to approximately 2.5V and R_{FBC} scales the large OUT1/OUT2 signal to down to 4Vpp.

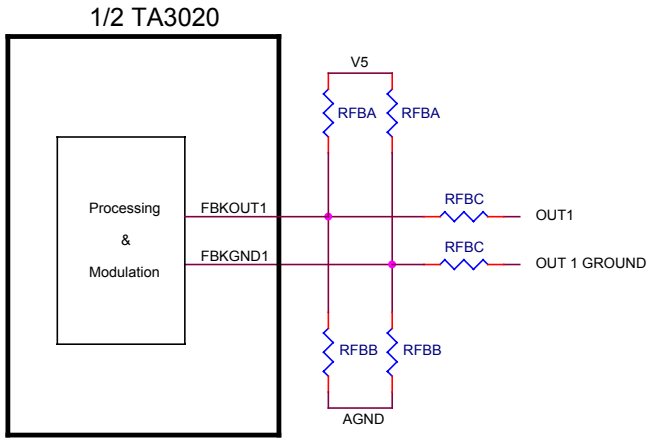


Figure 3: Modulator Feedback

The modulator feedback resistors are:

$$R_{FBA} = \text{User specified, typically } 1K\Omega$$

$$R_{FBB} = \frac{R_{FBA} * VPP}{(VPP - 4)}$$

$$R_{FBC} = \frac{R_{FBA} * VPP}{4}$$

$$A_{V\ -\ MODULATOR} \approx \frac{R_{FBC} * (R_{FBA} + R_{FBB})}{R_{FBA} * R_{FBB}} + 1$$

The above equations assume that VPP=|VNN|.

For example, in a system with VPP_{MAX}=52V and VNN_{MAX}=-52V,

R_{FBA} = 1kΩ, 1%
R_{FBB} = 1.08kΩ, use 1.07kΩ, 1%
R_{FBC} = 13.0kΩ, use 13.3kΩ, 1%

The resultant modulator gain is:

$$A_{V\ -\ MODULATOR} \approx \frac{13.3k\ \Omega * (1.0k\ \Omega + 1.07k\ \Omega)}{1.0k\ \Omega * 1.07k\ \Omega} + 1 = 26.73V/V$$

Mute

When a logic high signal is supplied to MUTE, both amplifier channels are muted (both high- and low-side transistors are turned off). When a logic level low is supplied to MUTE, both amplifiers are fully operational. There is a delay of approximately 200 milliseconds between the de-assertion of MUTE and the un-muting of the TA3020.

Turn-on & Turn-off Noise

If turn-on or turn-off noise is present in a TA3020 amplifier, the cause is frequently due to other circuitry external to the TA3020. While the TA3020 has circuitry to suppress turn-on and turn-off transients, the combination of the power supply and other audio circuitry with the TA3020 in a particular application may

exhibit audible transients. One solution that will completely eliminate turn-on and turn-off pops and clicks is to use a relay to connect/disconnect the amplifier from the speakers with the appropriate timing at power on/off. The relay can also be used to protect the speakers from a component failure (e.g. shorted output MOSFET), which is a protection mechanism that some amplifiers have. Circuitry external to the TA3020 would need to be implemented to detect these failures.

DC Offset

While the DC offset voltages that appear at the speaker terminals of a TA3020 amplifier are typically small, Tripath recommends that any offsets during operation be nulled out of the amplifier with a circuit like the one shown connected to IN1 and IN2 in the Test/Application Circuit.
It should be noted that the DC voltage on the output of a TA3020 amplifier with no load in mute will not be zero. This offset does not need to be nulled. The output impedance of the amplifier in mute mode is approximately 10KΩ. This means that the DC voltage drops to essentially zero when a typical load is connected.

HMUTE

The HMUTE pin is a 5V logic output that indicates various fault conditions within the device. These conditions include: over-current, overvoltage and undervoltage. The HMUTE output is capable of directly driving an LED through a series 2kΩ resistor.

Over-current Protection

The TA3020 has over-current protection circuitry to protect itself and the output transistors from short-circuit conditions. The TA3020 uses the voltage across a resistor R_S (measured via OCS1HP, OCS1HN, OCS1LP and OCS1LN) that is in series with each output MOSFET to detect an over-current condition. R_S and R_{OCR} are used to set the over-current threshold. The OCS pins must be Kelvin connected for proper operation. See "Circuit Board Layout" in Application Information for details.

When the voltage across R_{OCR} becomes greater than V_{TOC} (approximately 1.0V) the TA3020 will shut off the output stages of its amplifiers. The occurrence of an over-current condition is latched in the TA3020 and can be cleared by toggling the MUTE input or cycling power.

Setting Over-current Threshold

R_S and R_{OCR} determine the value of the over-current threshold, I_{SC}:

$$I_{SC} = 3580 \times (V_{TOC} - I_{BIAS} * R_{OCR})/(R_{OCR} * R_S)$$

$$R_{OCR} = (3580 \times V_{TOC})/(I_{SC} * R_S + 3580 * I_{BIAS})$$

where:
R_S and R_{OCR} are in Ω
V_{TOC} = Over-current sense threshold voltage (See Electrical Characteristics Table)
= 1.0V typically
I_{BIAS} = 20uA

For example, to set an I_{SC} of 30A, R_{OCR} = 9.63KΩ and R_S will be 10mΩ.

As high-wattage resistors are usually only available in a few low-resistance values (10mΩ, 25mΩ and 50mΩ), R_{OCR} can be used to adjust for a particular over-current threshold using one of these values for R_S.

It should be noted that the addition of the bulk C_{HBR} capacitor shown in the Application / Test Diagram will increase the I_{SC} level. Thus, it will be larger than the theoretical value shown above. Once the designer has settled on a layout and specific C_{HBR} value, the system I_{SC} trip point can be adjusted by increasing the R_{OCR} value. The R_{OCR} should be increased to a level that allows expected range of loads to be driven well into clipping without current limiting while still protecting the output MOSFETs in case of a short circuit condition.

Over- and Under-Voltage Protection

The TA3020 senses the power rails through external resistor networks connected to VNNSENSE and VPPSENSE. The over- and under-voltage limits are determined by the values of the resistors in the networks, as described in the table “Test/Application Circuit Component Values”. If the supply voltage falls outside the upper and lower limits determined by the resistor networks, the TA3020 shuts off the output stages of the amplifiers. The removal of the over-voltage or under-voltage condition returns the TA3020 to normal operation. Please note that trip points specified in the Electrical Characteristics table are at 25°C and may change over temperature.

The TA3020 has built-in over and under voltage protection for both the VPP and VNN supply rails. The nominal operating voltage will typically be chosen as the supply “center point.” This allows the supply voltage to fluctuate, both above and below, the nominal supply voltage.

VPPSENSE (pin 29) performs the over and undervoltage sensing for the positive supply, VPP. VNNSENSE (pin 30) performs the same function for the negative rail, VNN. When the current through $R_{VPPSENSE}$ (or $R_{VNNSENSE}$) goes below or above the values shown in the Electrical Characteristics section (caused by changing the power supply voltage), the TA3020 will be muted. VPPSENSE is internally biased at 2.5V and VNNSENSE is biased at 1.25V.

Once the supply comes back into the supply voltage operating range (as defined by the supply sense resistors), the TA3020 will automatically be unmuted and will begin to amplify. There is a hysteresis range on both the VPPSENSE and VNNSENSE pins. If the amplifier is powered up in the hysteresis band the TA3020 will be muted. Thus, the usable supply range is the difference between the over-voltage turn-off and under-voltage turn-off for both the VPP and VNN supplies. It should be noted that there is a timer of approximately 200mS with respect to the over and under voltage sensing circuit. Thus, the supply voltage must be outside of the user defined supply range for greater than 200mS for the TA3020 to be muted.

Figure 4 shows the proper connection for the Over / Under voltage sense circuit for both the VPPSENSE and VNNSENSE pins.

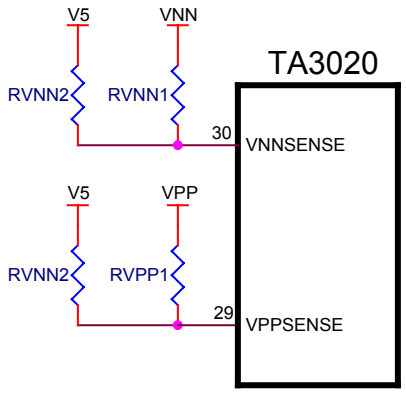


Figure 4: Over / Under voltage sense circuit

The equation for calculating R_{VPP1} is as follows:

$$R_{VPP1} = \frac{VPP}{I_{VPPSENSE}}$$

Set $R_{VPP2} = R_{VPP1}$.

The equation for calculating $R_{VNNSENSE}$ is as follows:

$$R_{VNN1} = \frac{VNN}{I_{VNNSENSE}}$$

Set $R_{VNN2} = 3 \times R_{VNN1}$.

$I_{VPPSENSE}$ or $I_{VNNSENSE}$ can be any of the currents shown in the Electrical Characteristics table for VPPSENSE and VNNSENSE, respectively.

The two resistors, R_{VPP2} and R_{VNN2} compensate for the internal bias points. Thus, R_{VPP1} and R_{VNN1} can be used for the direct calculation of the actual VPP and VNN trip voltages without considering the effect of R_{VPP2} and R_{VNN2}.

Using the resistor values from above, the actual minimum over voltage turn off points will be:

$$VPP_{MIN\_OV\_TUR\ N\_OFF} = R_{VPP1} \times I_{VPPSENSE\ (MIN\_OV\_TU\ RN\_OFF)}$$
$$VNN_{MIN\_OV\_TUR\ N\_OFF} = -(R_{VNN1} \times I_{VNNSENSE\ (MIN\_OV\_TU\ RN\_OFF)})$$

The other three trip points can be calculated using the same formula but inserting the appropriate $I_{VPPSENSE}$ (or $I_{VNNSENSE}$) current value. As stated earlier, the usable supply range is the difference between the minimum overvoltage turn off and maximum under voltage turn-off for both the VPP and VNN supplies.

$$VPP_{RANGE} = VPP_{MIN\_OV\_TUR\ N\_OFF} - VPP_{MAX\_UV\_TUR\ N\_OFF}$$
$$VNN_{RANGE} = VNN_{MIN\_OV\_TUR\ N\_OFF} - VNN_{MAX\_UV\_TUR\ N\_OFF}$$

VN10 Supply

VN10 is an additional supply voltage required by the TA3020. VN10 must be 10 volts more positive than the nominal VNN. VN10 must track VNN. Generating the VN10 supply requires some care.

The proper way to generate the voltage for VN10 is to use a 10V-postive supply voltage referenced to the VNN supply. Figure 5 shows the correct way to power the TA3020:

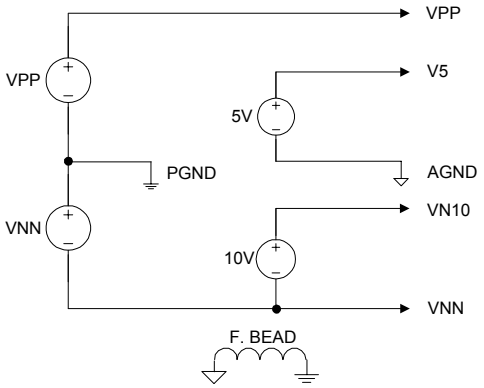


Figure 5: Proper Power Supply Connection

One apparent method to generate the VN10 supply voltage is to use a negative IC regulator to drop PGND down to 10V (relative to VNN). This method will not work since negative regulators only sink current into the regulator output and will not be capable of sourcing the current required by VN10. Furthermore, problems can arise since VN10 will not track movements in VNN.

Output Transistor Selection

The key parameters to consider when selecting what MOSFET to use with the TA3020 are drain-source breakdown voltage (BVdss), gate charge (Qg), and on-resistance ($R_{DS(ON)}$).

The BVdss rating of the MOSFET needs to be selected to accommodate the voltage swing between V_{SPOS} and V_{SNEG} as well as any voltage peaks caused by voltage ringing due to switching transients. With a 'good' circuit board layout, a BVdss that is 50% higher than the VPP and VNN voltage swing is a reasonable starting point. The BVdss rating should be verified by measuring the actual voltages experienced by the MOSFET in the final circuit.

Ideally a low Qg (total gate charge) and low $R_{DS(ON)}$ are desired for the best amplifier performance. Unfortunately, these are conflicting requirements since $R_{DS(ON)}$ is inversely proportional to Qg for a typical MOSFET. The design trade-off is one of cost versus performance. A lower $R_{DS(ON)}$ means lower $I^2R_{DS(ON)}$ losses but the associated higher Qg translates into higher switching losses (losses = Qg x 10 x 1.2MHz). A lower $R_{DS(ON)}$ also means a larger silicon die and higher cost. A higher $R_{DS(ON)}$ means lower cost and lower switching losses but higher I^2R_{DSON} losses.

The following table lists BVdss, Qg and $R_{DS(ON)}$ for MOSFETs that Tripath has used with the TA3020:

Manufacturer	Manufacturer's Part Number	BVdss	Qg (nanoCoulombs)	$R_{DS(ON)}$ (Max) (Ohms)
ST Microelectronics	STW34NB20	200	60	0.075
ST Microelectronics	STP19NB20	200	29	0.18
International Rectifier	IRFB41N15D	150	67	0.045
International Rectifier	IRFB31N20D	200	70	0.082
Fairchild	FQA34N20	200	60	0.075

Gate Resistor Selection

The gate resistors, R_G, are used to control MOSFET switching rise/fall times and thereby minimize voltage overshoots. They also dissipate a portion of the power resulting from moving the gate charge each time the MOSFET is switched. If R_G is too small, excessive heat can be generated in the driver. Large gate resistors lead to slower MOSFET switching, which requires a larger break-before-make (BBM) delay.

Break-Before-Make (BBM) Timing Control

The half-bridge power MOSFETs require a deadtime between when one transistor is turned off and the other is turned on (break-before-make) in order to minimize shoot through currents. BBM0 and BBM1 are logic inputs (connected to logic high or pulled down to logic low) that control the break-before-make timing of the output transistors according to the following table.

BM1	BBM0	Delay
0	0	120 ns
0	1	80 ns
1	0	40 ns
1	1	0 ns

Table 1: BBM Delay

The tradeoff involved in making this setting is that as the delay is reduced, distortion levels improve but shoot-through and power dissipation increase. Both the 40nS and 0nS settings are NOT recommended due the high level of shoot-thru current that will result. Thus, BBM1 should be grounded in most applications. All typical curves and performance information was done with using the 80ns or 120ns BBM setting. The actual amount of BBM required is dependent upon other component values and circuit board layout, the value selected should be verified in the actual application circuit/board. It should also be verified under maximum temperature and power conditions since shoot-through in the output MOSFETs can increase under these conditions, possibly requiring a higher BBM setting than at room temperature.

Output Filter Design

One advantage of Tripath amplifiers over PWM solutions is the ability to use higher-cutoff-frequency filters. This means load-dependent peaking/droop in the 20kHz audio band potentially caused by the filter can be made negligible. This is especially important for applications where the user may select a 4-Ohm or 8-Ohm speaker. Furthermore, speakers are not purely resistive loads and the impedance they present changes over frequency and from speaker model to speaker model.

Tripath recommends designing the filter as a 2nd order, 100kHz LC filter. Tripath has obtained good results with L_F = 11uH and C_F = 0.22uF.

The core material of the output filter inductor has an effect on the distortion levels produced by a TA3020 amplifier. Tripath recommends low-mu type-2 iron powder cores because of their low loss and high linearity (available from Micrometals, www.micrometals.com). The specific core used on the EB-TA3020 was a T106-2 wound with 29 turns of 16AWG wire.

Tripath also recommends that an RC damper be used after the LC low-pass filter. No-load operation of a TA3020 amplifier can create significant peaking in the LC filter, which produces strong resonant currents that can overheat the output MOSFETs and/or other components. The RC dampens the peaking and prevents problems. Tripath has obtained good results with R_D = 20Ω and C_D = 0.22uF.

Bridging the TA3020

The TA3020 can be bridged by returning the signal from OAOUT1 to the input resistor at INV2. OUT1 will then be a gained version of OAOUT1, and OUT2 will be a gained and inverted version of OAOUT1 (see Figure 6). When the two amplifier outputs are bridged, the apparent load impedance seen by each output is halved, so the current capability of the output MOSFETs, as well their power dissipation capability, must be accounted for in the design. In addition, the higher peak currents caused by driving lower impedance loads will cause additional ringing on the outputs. Thus, the layout and supply decoupling for low impedance (below 8 ohms) bridged applications must be extremely good to minimize output ringing and to ensure proper amplifier performance.

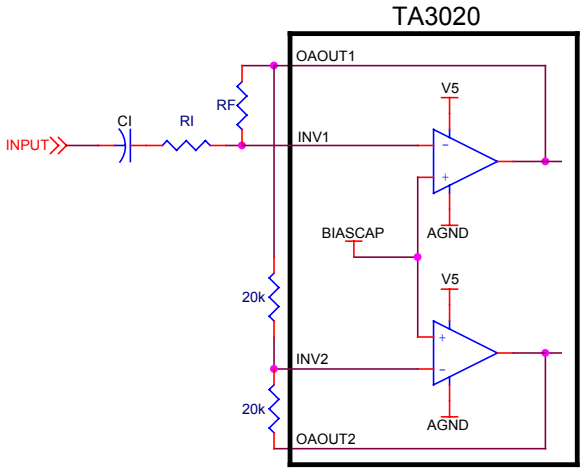


Figure 6: Input Stage Setup for Bridging

The switching outputs, OUT1 and OUT2, are not synchronized, so a common inductor may not be used with a bridged TA3020. For this same reason, individual zobel networks must be applied to each output to load each output and lower the Q of each common mode differential LC filter.

Low-frequency Power Supply Pumping

A potentially troublesome phenomenon in single-ended switching amplifiers is power supply pumping. This phenomenon is caused by current from the output filter inductor flowing into the power supply output filter capacitors in the opposite direction as a DC load would drain current from them. Under certain conditions (usually low-frequency input signals), this current can cause the supply voltage to "pump" (increase in magnitude) and eventually cause over-voltage/under-voltage shut down. Moreover, since over/under-voltage are not "latched" shutdowns, the effect would be an amplifier that oscillates between on and off states. If a DC offset on the order of 0.3V is allowed to develop on the output of the amplifier (see "DC Offset Adjust"), the supplies can be boosted to the point where the amplifier's over-voltage protection triggers.

One solution to the pumping issue it to use large power supply capacitors to absorb the pumped supply current without significant voltage boost. The low-frequency pole used at the input to the amplifier determines the value of the capacitor required. This works for AC signals only.

A no-cost solution to the pumping problem uses the fact that music has low frequency information that is correlated in both channels (it is in phase). This information can be used to eliminate boost by putting the two channels of a TA3020 amplifier out of phase with each other. This works because each channel is pumping out of phase with the other, and the net effect is a cancellation of pumping currents in the power supply. The phase of the audio signals needs to be corrected by connecting one of the speakers in the opposite polarity as the other channel.

Theoretical Efficiency Of A TA3020 Amplifier

The efficiency, η, of an amplifier is:

$$\eta = P_{OUT}/P_{IN}$$

The power dissipation of a TA3020 amplifier is primarily determined by the on resistance, R_{ON}, of the output transistors used, and the switching losses of these transistors, P_{SW}. For a TA3020 amplifier, P_{IN} (per channel) is approximated by:

$$P_{IN} = P_{DRIVER} + P_{SW} + P_{OUT}\,((R_S + R_{ON} + R_{COIL} + R_L)/R_L)^2$$

where: P_{DRIVER} = Power dissipated in the TA3020 = 1.6W/channel
$P_{SW} = 2 \times (0.01) \times Q_g$ (Q_g is the gate charge of M, in nano-coulombs)
R_{COIL} = Resistance of the output filter inductor (typically around 50mΩ)

For a 125W RMS per channel, 8Ω load amplifier using STW34NB20 MOSFETs, and an R_S of 50mΩ,

$$P_{IN} = P_{DRIVER} + P_{SW} + P_{OUT}\,((R_S + R_{ON} + R_{COIL} + R_L)/R_L)^2$$
$$= 1.6 + 2 \times (0.01) \times (95) + 125 \times ((0.025 + 0.11 + 0.05 + 8)/8)^2 = 1.6 + 1.9 + 130.8$$
$$= 134.3\text{W}$$

In the above calculation the $R_{DS\,(ON)}$ of 0.065Ω was multiplied by a factor of 1.7 to obtain R_{ON} in order to account for some temperature rise of the MOSFETs. ($R_{DS\,(ON)}$ typically increases by a factor of 1.7 for a typical MOSFET as temperature increases from 25ºC to 170ºC.)

So, $\eta = P_{OUT}/P_{IN} = 125/134.3 = 93\%$

Performance Measurements of a TA3020 Amplifier

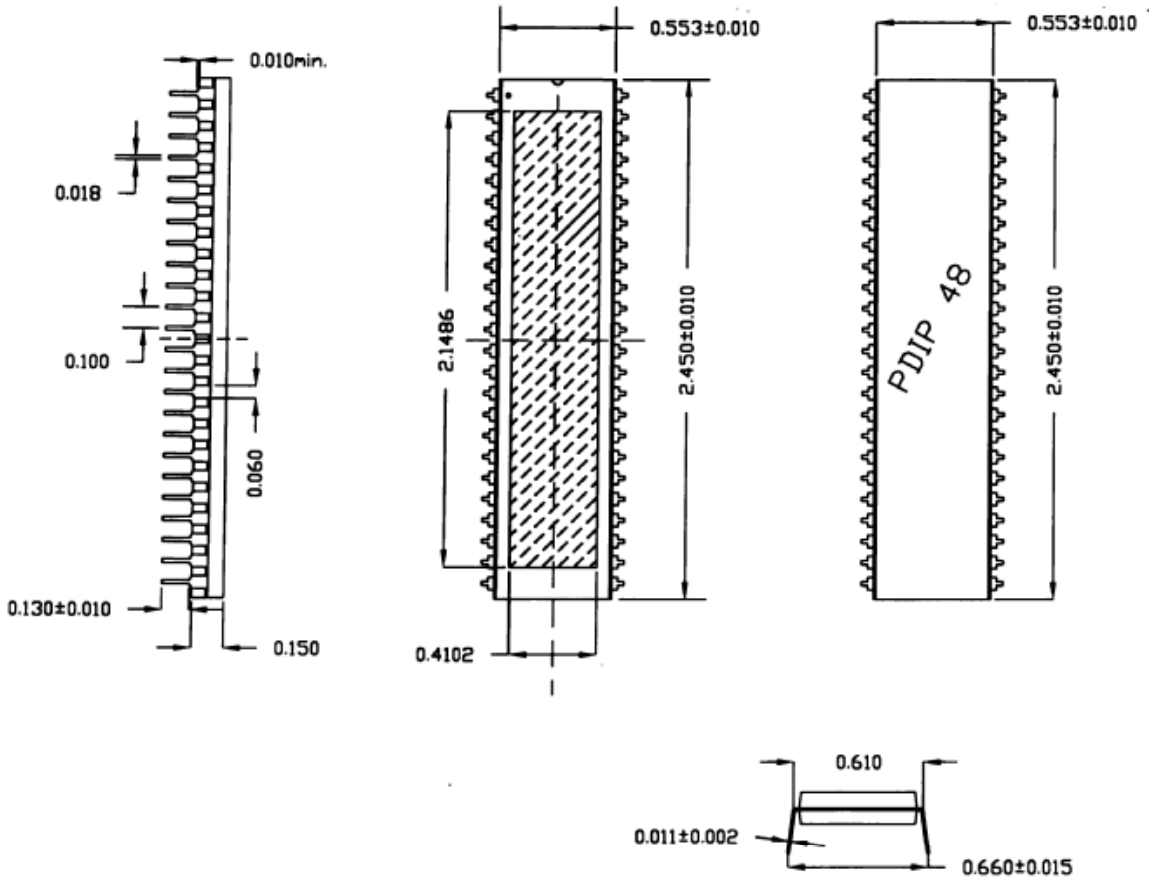
Tripath amplifiers operate by modulating the input signal with a high-frequency switching pattern. This signal is sent through a low-pass filter (external to the TA3020) that demodulates it to recover an amplified version of the audio input. The frequency of the switching pattern is spread spectrum and typically varies between 200kHz and 1.5MHz, which is well above the 20Hz – 22kHz audio band. The pattern itself does not alter or distort the audio input signal but it does introduce some inaudible noise components.

The measurements of certain performance parameters, particularly those that have anything to do with noise, like THD+N, are significantly affected by the design of the low-pass filter used on the output of the TA3020 and also the bandwidth setting of the measurement instrument used. Unless the filter has a very sharp roll-off just past the audio band or the bandwidth of the measurement instrument ends there, some of the inaudible noise components introduced by the Tripath amplifier switching pattern will get integrated into the measurement, degrading it.

Tripath amplifiers do not require large multi-pole filters to achieve excellent performance in listening tests, usually a more critical factor than performance measurements. Though using a multi-pole filter may remove high-frequency noise and improve THD+N type measurements (when they are made with wide-bandwidth measuring equipment), these same filters can increase distortion due to inductor non-linearity. Multi-pole filters require relatively large inductors, and inductor non-linearity increases with inductor value.

Package Information

48-pin DIP



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